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## A NEW REVERSIBLE VARACTOR FREQUENCY HALVER/DOUBLER DEVICE

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### ABSTRACT

A new reversible varactor frequency Halver/Doubler device is presented for the first time. The design approach is based on the analogy between frequency multipliers and dividers at the same steady state conditions. Hence, the well known design techniques for varactor doublers may be used for designing frequency halvers. Using this method a 8GHz to 4GHz halver was design and built. When reversed, the circuit functions as a doubler.

### INTRODUCTION

Parametric frequency dividers using varactors are useful in many system applications, due to their superior performance and much simpler circuit configuration as compared to other regenerative circuits. The basic theory of device operation is presented in [1,2]. Divider designs based on empirical techniques are described in [3,4], while analyzed in [5].

This work points out the analogy and equivalence between frequency multipliers and dividers from the design point of view.

The steady state operation of varactor doubler and halver circuits are described, leading to the same large signal equations and same dynamic impedances of the varactor in both circuits. It is shown that the circuit conditions necessary for frequency division fit the circuit configuration of varactor multipliers when run backwards [6].

A practical design of a varactor halver is presented, applying the well known design concepts for multipliers [7,9]. This approach results for the first time in a new reversible microwave Halver/Doubler device.

### ANALOGY BETWEEN DIVIDER AND MULTIPLIER CIRCUITS

When generating subharmonics of the driving frequency, varactors behave much like oscillators. As the output current builds up, nonlinear effects reduce the rate of amplitude rise and finally a steady state with a constant output power is reached.

For the divider circuit shown in Fig. 1a we assume that the currents are allowed to flow at only the driving frequency $f_p=2f_0$ and the output frequency $f_0$. A similar circuit is shown for a doubler in Fig. 1b, except that the driving source and load are interchanged.

The varactor is described by a nonlinear voltage-dependent junction capacitance $C_j$ and a series resistance $R_s$.

The well known expression for the $C_j$-v characteristics of the varactor is:

$$C_j=C_{min}\left(\frac{v+\phi}{V_B+\phi}\right)^{-\gamma} \qquad (1)$$

where:
- v - voltage across the junction
- $V_B$ - breakdown voltage
- $\phi$ - contact potential
- $\gamma$ - constant.

Although the principle of operation, and the transient and dynamic behavior of a doubler and a halver circuits are not the same, their steady state analysis as described in [2] and [6] are equivalent.

The steady state equations are large signal for the voltage $\hat{V}_1$ at $f_0$ and $V_2$ at $2f_0$ as functions of the currents $I_1$ at $f_0$ and $I_2$ at $2f_0$.

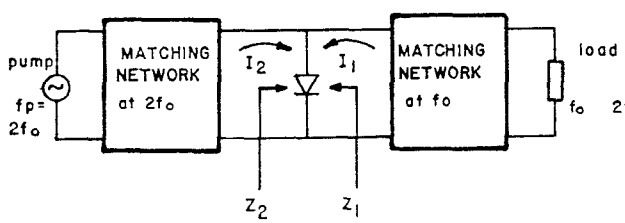


Fig. 1a: General description of a parametric frequency divider.

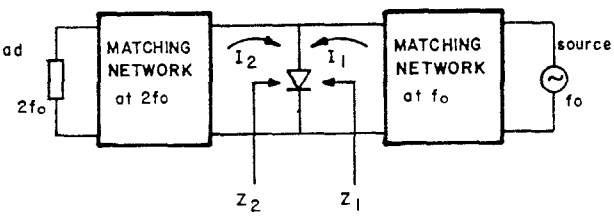


Fig. 1b: General description of a frequency multiplier.



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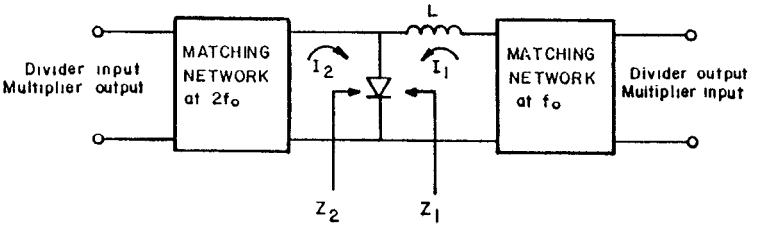


Fig. 2: General circuit of varactor multiplier or divider.

The same closed form steady state equations for the doubler and halver are obtained [2,6], analyzing the abrupt-junction varactor ($\gamma=\frac{1}{2}$).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} R_s + \frac{S_0}{j\omega_0} & \frac{S_1^*}{2j\omega_0} \\ \frac{S_1}{j2\omega_0} & R_s + \frac{S_0}{j2\omega_0} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2)$$

where $S_0$ and $S_1$ are Fourier coefficients, and $S=1/C_j$.

Let $Z_1$ and $Z_2$ be the dynamic impedances of the varactor at $f_0$ and $2f_0$ as defined in Fig. 1a,b.

Then:

$$V_1=Z_1I_1 \quad (3)$$

$$V_2=Z_2I_2 \quad (4)$$

This treatment leads to the same closed form solution for $Z_1$ and $Z_2$ in a doubler or a halver (the same is true for the bias voltage, efficiency etc.). In principle the same concept holds for other types of varactors of different characteristics.

The normalized optimal varactor impedances for multipliers design which depend on the $\gamma$ of the $C_j$-v characteristics and drive level, are presented in [7,8]. Therefore, from the steady state operation point of view those parameters may be useful for designing frequency dividers.

In [6] the conditions for frequency division to occur in a varactor is discussed. It has been found that the circuit condition to support growing oscillations is the requirement of an inductance L which resonates the varactor average capacitance at the subharmonic output frequency. However such an inductor exists also in multiplier circuits [9], as described in Fig. 2.

Hence, doubler's design techniques and circuit configuration seem to be a practical efficient solution for application in dividers design.

## A DESIGN EXAMPLE OF A MICROWAVE HALVER

To demonstrate the proposed method, a design of a microwave halver is described. The circuit was designed by applying doubler's design methods, for the required input frequency of 8GHz.

The circuit consists of an input network which should act as a matching network of the band-pass type, providing also isolation between the pump signal and the signals generated by the diode.

This network is an interdigital type which covers the required few percent bandwidth centered at 8GHz.

The output matching network is a comb-line type, which passes only the output frequency $f_0$. The input/output networks match the low impedances of the varactor to 50Ω at the input and output frequencies.

Those dynamic impedances are calculated from given table for doublers [7].

The design of the matching input/output networks is accomplished by a simple straightforward CAD, using the circuit topology shown in Fig. 3.

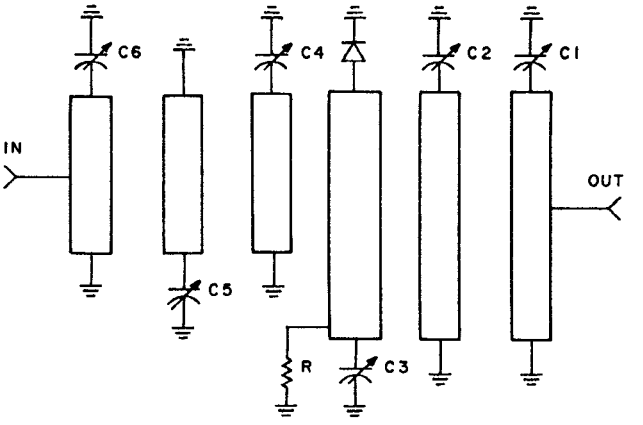


Fig. 3: Divider's electronic circuit drawing.

The diode used in this example is a step-recovery device, with a self bias arrangement.

The circuit was built in a coaxial structure, in which tuning screws were used to tune the circuit for optimum performance.

## MEASURED RESULTS OF THE HALVER

A minimum level of input power $P_{in}$ is required, in order for frequency division to occur. For this divider the threshold input level is about 12dBm,

at which frequency division commences abruptly at a narrow band. As $P_{in}$ increases beyond this level, the bandwidth is increases.

The output frequency response of the divider, tested at $P_{in}$=18dBm(±½dB) is shown in Fig. 4.

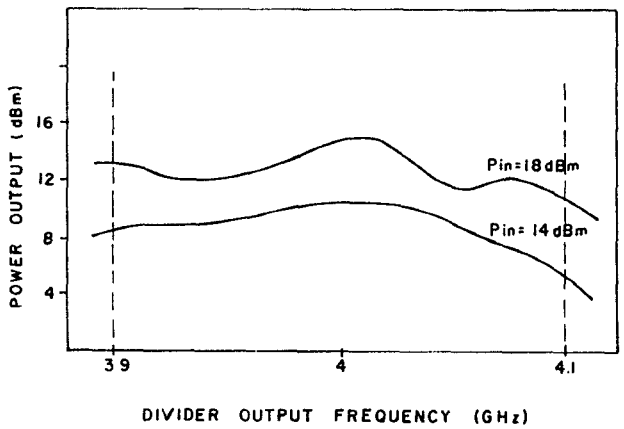


Fig. 4: Frequency response at $f_0=\frac{1}{2}f_{in}$ and dynamic range behavior of the divider.

As shown, a reasonable conversion loss of 3 to 6dB is obtained, over a bandwidth of about 4 percent. The only measured spurius signal at the output is at $f_{in}$, which was about 45dB below the $\frac{1}{2}f_{in}$ output signal.

## REVERSIBLE CHARACTERISTICS OF THE DEVICE

The halver circuit was tested as a doubler by reversing its input/output ports. It is interesting to point out, that the circuit functioned as a doubler of similar conversion loss and same bandwidth as the halver, without any retuning. Its performance as a doubler is shown in Fig. 5.

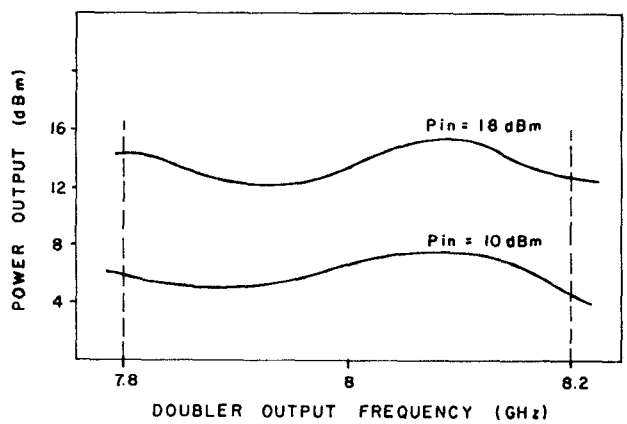


Fig. 5: Frequency response and dynamic range of the reversed halver circuit tested as a doubler (without retuning).

The main difference in performance between the two functions of the circuit is the dynamic range behavior. As a doubler the circuit has a much wider dynamic range and there is no threshold level of input power as observed for the halver.

The output power versus input power for the design example, tuned as a halver and tested as both a halver and a doubler is shown in Fig. 6.

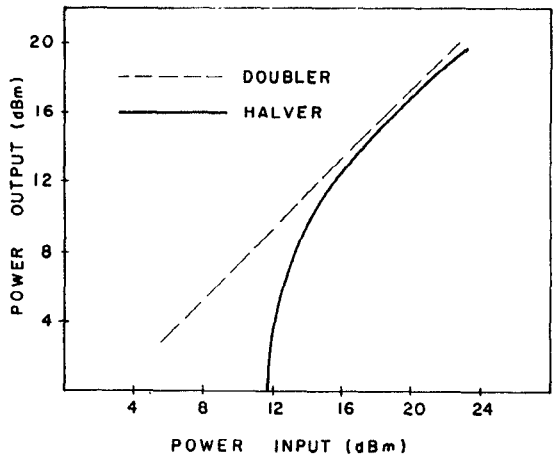


Fig. 6: Output power versus input power for the circuit, tested as both a halver and a doubler.

Concerning the reversible characteristics of the circuit, it was found that tuning it as a halver results in a reversible device. On the other hand, tuning it as a doubler (by reversing its in/out ports) for max. efficiency, the circuit will not function reversal, unless the required conditions [6] for frequency division to occur in a varactor, are fulfilled. Hence, the reversible characteristics behavior of the circuit is conditional.

## CONCLUSIONS

A practical approach for the design of a microwave frequency divider has been demonstrated. The design method is based on the analogy between multipliers and dividers, applying the existing design techniques and circuit configuration for doublers, for the design of halvers. Using this method, a 8GHz to 4GHz halver was design and built. This approach results for the first time in a new reversible microwave halver/doubler device.


## ACKNOWLEDGMENT

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